



# UNITED STATES PATENT AND TRADEMARK OFFICE

*per*  
UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,443	12/05/2003	Stephen Gordon	SDV-001A	1072
23446 7590 08/09/2007 MCANDREWS HELD & MALLOY, LTD 500 WEST MADISON STREET SUITE 3400 CHICAGO, IL 60661			EXAMINER TAYONG, HELENE E	
			ART UNIT 2611	PAPER NUMBER
			MAIL DATE 08/09/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/729,443	<b>Applicant(s)</b> GORDON ET AL.	
	<b>Examiner</b> Helene Tayong	<b>Art Unit</b> 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 5/31/07.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is in response to the amendment filed on May 31, 2007. Claims 1-17 are presently pending. Claims 1-15 stand rejected. Claims 16 and 17 are added. Claims 1-4 and 8-12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Linzer. Claims 5 and 13 were rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Linzer in view of Ju. Claims 6, 7, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Linzer in view of Lavelle. Additionally, Examiner objected to claim 9. Claim 9 is amended, and it is believed that claim 9 overcomes Examiner's objection. Claims 1-17 are pending in this application and have been considered below.

### ***Response to Arguments***

2. Applicants arguments regarding the rejection under 35 USC 102(e) as being anticipated by Linzer et al. (US Publication Number 2004/0100577 A1) have been fully considered but they are not persuasive. The examiner thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meets the claimed limitation as rejected.

**(1) Applicant's arguments:** " Linzer does not teach A method ... comprising .... storing data in a machine readable memory device a first time at a first memory address;" and "storing the data in the machine readable memory device a second time at a second memory address"

**The examiner's response:** Fig. 5A and 5B illustrate a memory comprising a storage device. One of ordinary skill in the art would have clearly recognized the two memory addresses (left and right addresses shown on Fig. 5A and 5B as storage addresses). Further, on page 2, [0020], memory (102) which is interpreted as Machine readable medium is disclosed to store data in both memory addresses. It would have been obvious to one of ordinary skill in the art at the time of the invention to consider the memories to storing data in a machine readable memory device a first time at a first memory address, and storing the data in the machine readable memory device a second time at a second memory address.

**(2) Applicant's arguments:** "The foregoing does not even teach "a second address", nor its particular "alignment with respect to the burst boundaries", much less "storing the data in the machine readable memory device a second time at a second memory address, the second memory address having a second alignment with respect to the burst boundaries" "

**The examiner's response:** On page 4 [0033] lines 14-17), Linzer et al. discloses "a burst may comprise 8 bytes to an 8 byte boundary from each of the memory chips". One of ordinary skill in the art would have considered the word **each** to mean the first and the second memory having alignment with respect to the burst boundaries.

Applicants are reminder that the Examiner is entitled to give the broadest reasonable interpretation to the language of the claim. So the Examiner considers "Machine Readable Memory Device" are "the first memory" and "the second memory" within the broad meaning of the term. The examiner is not limited to Applicant's definition, which is not specifically set fourth in the claims. *In re tanaka et al.*, 193 USPQ 139, (CCPA) 1977.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1- 4 , 8-12 and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Linzer at al. (US 2004/0100577 A1).

As shown in figure 5A, Linzer et al discloses an apparatus and method for storing image data.

(1) with regards to claim 1:

storing data in a machine readable memory device (interpreted as any RAM) a first time at a first memory address ( pg. 1, [0007], lines 3-6);

the machine readable memory device (SDRAM) having one or more burst boundaries (pg. 3, [0033], lines 11-14);

and the first memory address having a first alignment with respect to the burst boundaries (pg. 4, [0033], lines 12-14);

storing the data in the machine readable memory device a second time at a second memory address, the second memory address having a second alignment with respect to the burst boundaries (pg. 4, [0040], lines 1-6).

(2) with regards to claim 2:

wherein the data represents at least one reference frame (interpreted as DATA) for use in a video decoder (pg. 2, [0020], lines 4-5).

(3) with regards to claim 3:

wherein the video decoder is an h.264 codec (pg. 2, [0021], lines 1-2).

(4) with regards to claim 4:

wherein the machine readable memory device comprises volatile memory (interpreted as any RAM) (pg. 3, [0033], lines 1-3).

(5) with regards to claim 8:

storing the data in the machine readable memory device a third time at a third memory address, the third memory address having a third alignment with respect to the burst boundaries (pg. 6, Table 6A, [0055], lines 1-3).

(6) with regards to claim 9:

determining a set of desired bytes of data, the set of desired bytes of data having been previously stored in a machine readable memory device at two or more memory addresses, the memory device having at least one burst boundary, and each memory address having a different alignment with respect to the at

least one burst boundary (pg. 6, [0051], lines 1-5);

and retrieving the desired bytes of data from a preferred the memory address, the preferred memory address being aligned with the at least one burst boundary such that the number of bursts necessary to read the desired bytes from the preferred memory address is fewer than the number of bursts necessary to read the desired bytes from the other memory addresses ( pg.8, [0061], lines 1-10).

(7) with regards to claim 10:

wherein the data represents at least one reference frame (interpreted as DATA) for use in a video decoder (pg. 2, [0020], lines 4-5).

(8) with regards to claim 11:

wherein the video decoder is an h.264 codec (pg. 2, [0021], lines 1-2).

(9) with regards to claim 12:

wherein the machine readable memory device comprises volatile memory (interpreted as any RAM) (pg. 3, [0033], lines 1-3).

(10) with regards to claim 16;

Linzer et al discloses in fig. 4 , 102, a circuit ( pg. 2, [0018] lines 4) for managing bursts of data, the method comprising:

a machine readable memory device for storing data (102) starting at a first memory address that has a first alignment with respect to burst boundaries, and concurrently storing the data starting at a second memory address that has a second alignment with respect to the burst boundaries ( pg. 2, [0020], 7-17) and (pg7, [0056]); and

a circuit for writing the data to the machine readable memory device a first time starting at the first memory address that has the first alignment with respect to the burst boundaries and writing the data in the machine readable memory device a second time starting at the second memory address that has the second alignment with respect to the burst boundaries ( see abstract lines 2-8), pages 3-4 , [0033], lines 11-17) and [0040]).

(11) with regards to claim 17;

Linzer et al discloses in fig. 4 , 102, a circuit ( pg. 2, [0018] lines 4) for managing bursts of data, said circuit comprising:

a machine readable memory device for storing data starting at a first memory address (102) that has a first alignment with respect to burst boundaries ( pg. 3, [0033], lines 11-14, and concurrently storing the data starting at a second memory address that has a second alignment with respect to the burst boundaries ( pages 3-4 , [0033], lines 11-17) and [0040]).; and

a circuit for determining a first number of bursts for retrieving the data (pg. 2, [0020], lines 2-6) from the first address (102) and determining a second number of bursts for retrieving the data from the second address and retrieving the data from the first address if the first number of bursts is fewer than the second number, and retrieving the data from the second address if the second number of bursts is fewer than the first number ( fig. 5B, pg. 2, [0022] -[0023] and pg. 3, [0032] lines 1-6).



Art Unit: 2611

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Linzer et al. in view of Ju et al. (US 2004/0155883 A1).

(1) with regards to claim 5:

Linzer et al. further discloses a memory video Data storage (102, fig. 5A).

Linzer et al. further discloses all of the subject matter as described above except the volatile memory is one of static random access memory (SRAM) and dynamic random access memory.

However, Ju et al. in the same field of endeavor, teaches the volatile memory is one of static random access memory (SRAM) and dynamic random access memory (DRAM) (pg2, [0023], lines 3-4).

One of ordinary skill would have clearly recognized that to use a memory that has large storage space, several banks and each bank includes many memory pages a DRAM would have been preferred and a memory that is much faster, a SRAM would have been preferred. To obtain high performance, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the memory in Linzer et al. with the volatile memory (content in memory is lost when power goes off), SRAM and DRAM of Ju et al. to easily store and retrieve data.

(2) with regards to claim 13:

same as in claim 5 above.

7. Claims 6,7,14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Linzer et al. in view of Lavelle et al. (US 2002/0171653 A1).

(1) with regards to claim 6:

Linzer et al. disclose all of the subject matter as described above except for the machine readable memory device comprises a non-volatile memory (ROM).

However, Lavelle et al. in the same field of endeavor, teaches the machine readable memory device comprises non-volatile memory (ROM) (pg. 4, [0054, lines 10-11).

One of ordinary skill would have clearly recognized that the internal ROM of a computer system stores at least boot-up code to boot-up the computer system at start up execution. To obtain faster execution performance and store (read only data) for an indefinite period of time, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the non-volatile memory (ROM) of Lavelle et al. in place of the memory in Linzer et al to boot system incase of failure.

(2) with regards to claim 7:

same as in claim 6 above.

(3) with regards to claim 14:

same as in claim 6 above.

(4) with regards to claim 15:

same as in claim 6 above.

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helene Tayong whose telephone number is 571-270-1675. The examiner can normally be reached on monday-Friday.

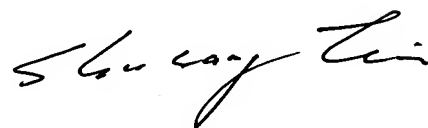
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lui Shuwang can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2611

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helene Tayong

8/6/07

A handwritten signature in black ink, appearing to read "Shuwang Liu", is positioned above the printed name and title.

**SHUWANG LIU**  
**SUPERVISORY PATENT EXAMINER**